Self-Aligned U-Gate Carbon Nanotube Field-Effect Transistor with Extremely Small Parasitic Capacitance and Drain-Induced Barrier Lowering

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ABSTRACT A novel self-aligned U-gate structure for carbon nanotube (CNT) field-effect transistors (FETs) is introduced and shown to yield excellent dc properties and high reproducibility that are comparable with that of the best CNT FETs based on the previously developed self-aligned device structures. In particular the subthreshold swing of the U-gate FET is 75 mV/dec and the drain-induced barrier lowering is effectively zero, indicating that the electrostatic potential of the whole CNT channel is most efficiently controlled by the U-gate and that the CNT device is a well-behaved FET. Moreover the high-frequency response of the U-gate FET is investigated, and the parasitic capacitance of the device is measured and shown to be one magnitude smaller than that of the previously developed self-aligned device structures. Direct frequency domain measurements show that the U-gate CNT FETs can operate up to 800 MHz, which is also higher than previously reported values. The large improvement in the device high-frequency behavior is largely due to the replacement of the high-κ dielectric material between the source/drain and the gate by a vacant space with $\kappa \approx 1$, and the significant reduction in the device parasitic capacitance renders the U-gate CNT FETs promising for rf applications.

KEYWORDS: carbon nanotube · field-effect transistor · self-aligned · high-speed circuit · parasitic capacitance

The carbon nanotube (CNT) has been considered as one of the most prevailing materials for building nanoelectronic devices.[1−3] This is mainly due to the perfect combination of its small size, extremely high carrier mobility, large current density, small intrinsic gate delay, and high intrinsic cutoff frequency.[4] After more than a decade of extensive investigations, the semiconducting CNT-based p-type and n-type field-effect transistors (FETs) have been shown to exhibit outstanding intrinsic properties and outperform the conventional Si-based MOSFET devices in several important aspects.[5−12] To continuously scale down the device dimensions, thus improving the device performance and increasing packing density, an optimized self-aligned (SA) procedure must be adopted to fabricate top-gate CNT FETs.[9,10,13] The SA procedure uses the predefined top-gate stack as the mask to automatically align the source and drain and thus significantly reduce the degree of gate overlapping with the source and drain, providing a reliable way to fabricate small FETs with small parasitic capacitance. Two distinct types of SA gate structures have been demonstrated for CNT FETs, pushing the dc performance of the CNT devices to the ballistic limit for both p-type[10] and n-type[9] CNT FETs, respectively. In addition, the intrinsic gate delay of sub-100 nm CNT devices fabricated using either type of SA structure has been demonstrated to be less than 1 ps, suggesting potential applications of the CNT devices in the THz regime. However, the experimentally measured cutoff frequency for the CNT device falls still far below the intrinsic performance limit, and this is mainly due to the existence of a large parasitic capacitance between the source/drain and gate electrodes, which is typically 3 orders of magnitudes larger than the intrinsic gate capacitance of the CNT device.[14] While this situation may be improved by adopting a dense parallel CNT array as the transistor channel,[14−16] there remains much room for reducing the parasitic capacitance and improving the rf performance of the CNT FET *via* optimizing the geometry of the device. It should be noted that in all previously published SA device structures,[9,10] there exists a high-κ dielectric layer (Al_2O_3 or HfO_2) between the gate and source/drain, and this high-κ dielectric layer significantly enlarges the parasitic capacitance (by a factor of $\sim\kappa$, with κ being the

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dielectric constant of the dielectric layer). Here we show that by utilizing a U-shaped top-gate geometry, the high-κ dielectric layer between the source/drain and gate electrodes can be replaced by a vacant space with $\kappa \approx 1$, thus reducing significantly the parasitic capacitance. Compared to the previously developed SA gate structures, the U-gate device exhibits not only excellent dc characteristics but also extremely small drain-induced barrier lowering (DIBL) and parasitic capacitance, suggesting that the U-gate CNT FETs are promising for high-speed and rf applications.

The self-aligned U-gate structure for a CNT FET and detailed fabricating process are shown in Figure 1. A strip of Y_2O_3/Ti gate stack was first fabricated (Figures 1a−d) and then used as the mask of deposition to separate the source and drain automatically from the U-shaped top-gate. The distinct feature of the U-gate is that the gate stack bends up at its two ends (Figure 1d), so that the source and drain electrodes are automatically separated vertically from the gate metal strip (Ti/Sc) on top of the gate stack; that is, the process is self-aligned. The CNT channel between the source and drain may be divided into three segments (Figure 1f): the middle part, which is covered directly by the gate oxide, and the two end regions, which are "ungated" (*i.e.*, not directly covered by the gate oxide), each with a length of L_{ug}. The source (drain) is separated from the top-gate by a vacant space as a result of the bending up of the gate stack toward the end. Unlike the previously developed SA gate structures,[9,10] the "ungated" segment of the CNT channel is not strictly ungated by the top-gate. Instead, the dielectric between the top-gate and the ungated CNT channel becomes a composite one that is composed of a thin layer of high-κ material and a low-κ (vacant) space with increasing thickness toward the source and drain. The gate control on the "ungated" CNT segment is not completely lost, but the gate efficiency is reduced. The gain achieved here, partially by losing control of the "ungated" part of the CNT channel, is the significantly reduced parasitic capacitance between the gate and source/drain, and this is of crucial importance for the development of CNT-based rf devices.

The SA U-gate CNT FETs were fabricated on an ultralong semiconducting CNT with a diameter d = 2.4 nm. For a typical device, the total channel length (between the source and drain) is about 600 nm, the ungated channel length L_{ug} is about 80 nm (Figure 1f), and the top-gated channel length is L_g = 600 − (2 × 80) = 440 nm (Figure 2a). In principle, L_{ug} may be controlled by varying the thickness and sensitivity of the bilayer resists (Figure 1a). In Figure 2a the white line contrast results from a semiconducting CNT and the red strip is due to a 0.6 μm gate electrode that separates automatically the source/drain electrodes (marked in yellow in Figure 2a). Shown in Figure 2b and c are dc characteristics for the Sc-contacted U-gate

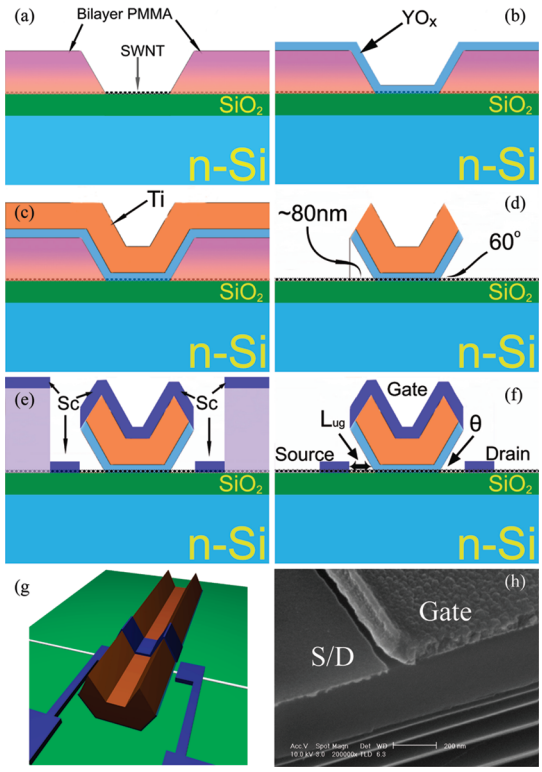

Figure 1. Self-aligned U-gate process. (a) A bilayer resist with continuously varying sensitivity is used for defining the U-shaped top-gate stack. (b) A 3 nm yttrium film is deposited by electron beam evaporation (EBE) and oxygenized to form a 6.5 nm Y_2O_3 gate dielectric. (c) A 70 nm Ti film is deposited by EBE. (d) A standard lift-off process is used to form the U-shaped top-gate electrode. The top-gate stack bends up toward the two ends, leaving two vacant spaces at its two ends. The horizontal dimension of the vacant space (or ungated area) is about 80 nm, and the bending angle is about 60°. (e) A second EBL process is used to define the source/drain window, and a 20 nm Sc is deposited. (f) A cross-sectional view of the U-shaped top-gate CNT FET geometry. (g) A prospective view of the device geometry. (h) SEM image showing a typical U-shaped self-aligned top-gate structure.

device. The Sc electrode is known to form a perfect ohmic contact to the conduction band of the CNT, providing a barrier-free channel for the electron injection into the CNT FET.[7] The gate transfer characteristics (Figure 2b) were obtained by sweeping the top-gate voltage from 2 to −2 V at different V_{ds}, and the three curves correspond respectively to 0.1 V (black), 0.3 V (red), and 0.5 V (blue). The current on/off ratio I_{on}/I_{off} reaches up to 10^5 at V_{ds} = 0.1 V and remains larger than 10^4 at V_{ds} = 0.5 V. The outstanding on-state properties of the device are manifested by the high saturation current of about 30 μA (Figure 2c) and the large transconductance g_m (Figure 2d), which shows a peak value of up to 23 μS at V_{gs} = −0.14 V and V_{ds} = 1.0 V. It is worth noting that the subthreshold swing $S = \partial V_{gs}/\partial(\log I_{ds})$ of about 75 mV/dec (Figure 2b) is also among the best that have been achieved for CNT FETs,[6,9] and this is largely due to the high efficiency of the top-gate originating from the use of the thin high-κ Y_2O_3 gate

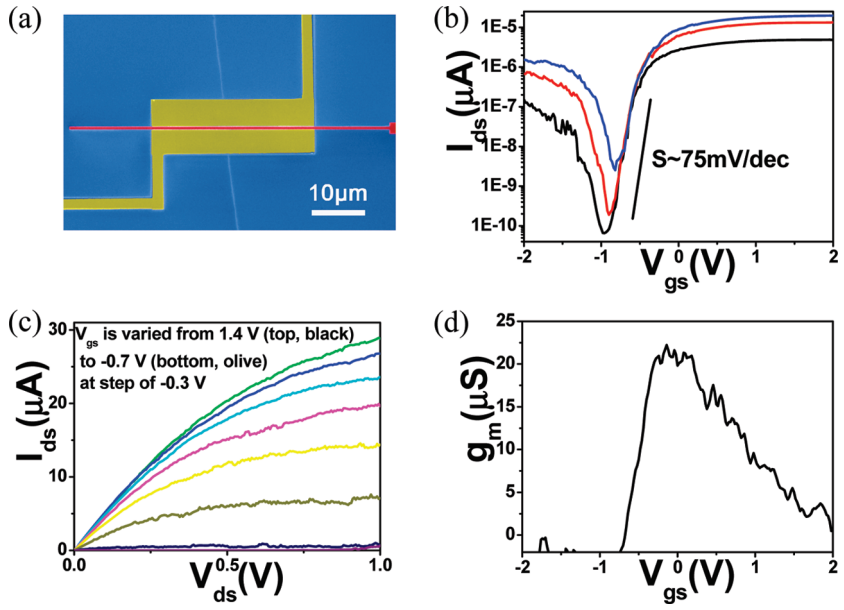

Figure 2. Geometry and dc characteristics of a self-aligned U-gate CNT FET. (a) SEM image showing a top view of the CNT FET. The thin red strip is the gate, the regions marked in yellow are the source and drain, and the white line in the middle is a single-walled CNT with a channel length $L_g \approx 0.6\ \mu$m and a diameter $d \approx 2.4$ nm. (b) Transfer characteristics for $V_{ds} = 0.1$ V (black), 0.3 V (red), and 0.5 V (blue), respectively, from bottom to top. (c) Output characteristics of the device with V_{gs} being varied from 1.4 V (top, black) to −0.7 V (bottom, olive) with a step of −0.3 V. (d) Gate voltage dependent transconductance g_m under $V_{ds} = 1.0$ V.

dielectric here.[17] Another important metric benchmarking the gate efficiency is DIBL.[18] For a well-designed transistor the gate capacitance should dominate so that the source and drain voltage have little effect on the potential profile near the top of the potential barrier along the conduction channel. For the state-of-the-art Intel 32 nm logic technology, the subthreshold slope of the FET is about 100 mV/dec, and DIBL is about 130 mV/V for n-type FET and 160 mV/V for p-type FET.[19] For our U-gate device, Figure 2b shows that DIBL is effectively zero, showing that the U-gate device is a well-behaved FET in which the electrostatic potential of the whole CNT channel is most efficiently controlled by the U-gate. Moreover, the reproducibility of the CNT devices is very high, benefitting from the self-aligned gate structure. For example, we have fabricated 20 devices on the same CNT, and 19 devices worked well, suggesting a high device yield of 95%.

The efficiency of the U-shaped top-gate on the CNT channel can also be investigated by studying the effect of the back gate on the transport properties of the top gate. Shown in Figure 3a are the top-gate transfer characteristics, which were obtained with the back gate being floated (black line) and being biased with $V_{bg} = 20$ V (red line). The same characteristics are also given in Figure 3b but in linear scale, showing clearly that the threshold voltage of the device V_{th} was shifted by about 130 mV toward the negative direction, *i.e.*, from 0.14 to 0.01 V, when the back gate was biased by 20 V. When the back gate was biased with 20 V, the transfer characteristic of the U-shaped top-gate shows clearly a larger off-state current than that when the back-gate was floated. The enhancement in the p-type and off-state current under positive V_{bg} may be attributed to the fact that the potential barrier for hole injection is reduced in the ungated segment of the CNT channel, leading to a higher hole injection efficiency. We therefore conclude that the dc properties of the U-gate device are comparable to those of the best published CNT FETs with optimized SA structures without the need of using the back-gate; that is, the device structure is well-designed and suitable for high-performance CNT FETs.

Finger-structured FETs can deliver large on-state current and are investigated for rf power amplifications.[10,20] The structure and performance of a multifinger CNT FET consisting of an array of 10 U-gate CNT FETs in parallel are shown in Figure 4. On one side of the CNT all electrodes are linked together as the source, while on the other side all electrodes are linked together as the drain (marked in yellow in Figure 4a). Between every adjacent pair of source and drain, the SA gate (red) was fabricated and linked together to serve as a common gate. In this structure (Figure 4a), multiple Sc-contacted U-gate CNT FETs are connected in parallel. The transfer characteristics of the device are shown in Figure 4b for $V_{ds} = 0.1$ V (black), 0.3 V (red), 0.5 V (blue), and 1 V (cyan), respectively. One of the advantages of this finger-structured device is that it can deliver a large on-state current of over 140 μA (Figure 4c), while Figure 4b shows that its off-state current remains very small (~30 pA), yielding a large current on/off ratio I_{on}/I_{off} of up to 10^5 even at $V_{ds} = 0.5$ V. The subthreshold swing S of about 75 mV/dec (Figure 4b) and DIBL of ~0 mV/V

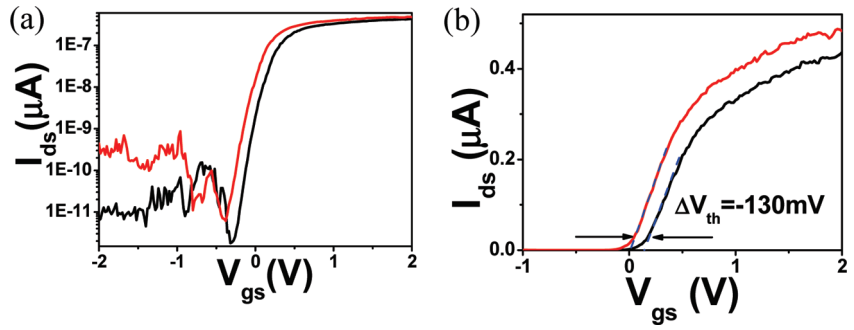

Figure 3. Transfer characteristics (a) in logarithmic scale and (b) in linear scale for a self-aligned U-gate CNT FET with the back-gate being floated (black) and being biased by V_{gs} =20 V (red). The length of the channel is about 0.8 μm, and the device is biased at V_{ds} = 0.1 V.

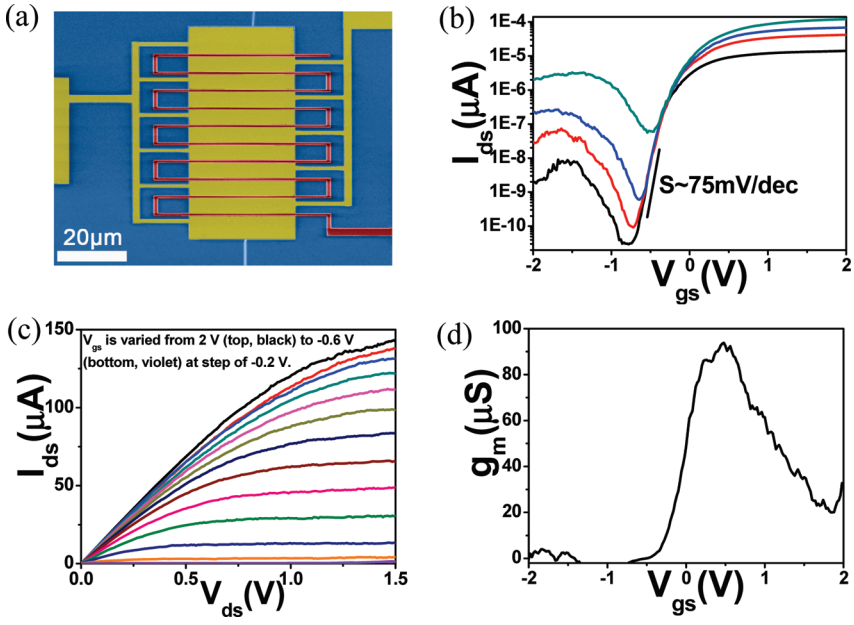

Figure 4. Geometry and dc characteristics of a finger-structured U-gate CNT FET. The device was fabricated on the same CNT as that shown in Figure 2, consisting of 10 channels each with a length of about 0.5 μm. (a) SEM image showing a top view of the finger-structured CNT FET. The thin red strip is the gate, the regions marked in yellow are the source and drain, and the white line in the middle is a single-walled CNT with a diameter $d \approx$ 2.4 nm. (b) Transfer characteristics for V_{ds} = 0.1 V (black), 0.3 V (red), 0.5 V (blue), and 1.0 V (dark cyan), respectively, from bottom to top. (c) Output characteristics of the device with V_{gs} being varied from 2 V (top, black) to −0.6 V (bottom, violet) with a step of −0.2 V. (d) Gate voltage dependent transconductance g_m under V_{ds} = 1.0 V.

are similar to that shown in Figure 2b for a single device. The coincidence of the subthreshold swing between the finger-structured FET and its single constituent FET demonstrates that all its 10 constituent FETs have very similar threshold voltages and subthreshold swing slopes. The peak transconductance g_m is up to 94 μS (Figure 4d) at V_{gs} = 0.48 V and V_{ds} = 1.0 V.

The operation speed of a FET is ultimately characterized by its cutoff frequency.[21] This key parameter can be obtained through standard *S*-parameter measurement using a network analyzer. However, it should be noted that the standard *S*-parameter measurement cannot be applied to accurately measure the frequency response of a single CNT FET in which the output resistance is much larger than 50 Ω, the ideal value for an impedance-matched measurement. Shown in Figure 5a is a general rf equivalent circuit model for a CNT FET. Using this model, the cutoff frequency of the CNT FET can be estimated as[4,14,21]

$$f_T \approx \frac{g_m}{2\pi(C_{gs} + C_{p,gd} + C_{p,gs})} \quad (1)$$

where g_m is the transconductance, C_{gs} is the gate capacitance, and $C_{p,gd}$ and $C_{p,gs}$ are the parasitic gate-drain and gate-source capacitances of the CNT device. The intrinsic cutoff frequency of the device is given by $g_m/2\pi C_{gs}$, assuming zero parasitic capacitance $C_{p,gd} = C_{p,gs} = 0$. Equation 1 shows clearly that the effective cutoff frequency is reduced by the parasitic capacitances $C_{p,gd}$ and $C_{p,gs}$. The transconductance g_m can be estimated from the dc transfer characteristic of the device (see, for example, Figure 2d), and C_{gs} can be calculated using the

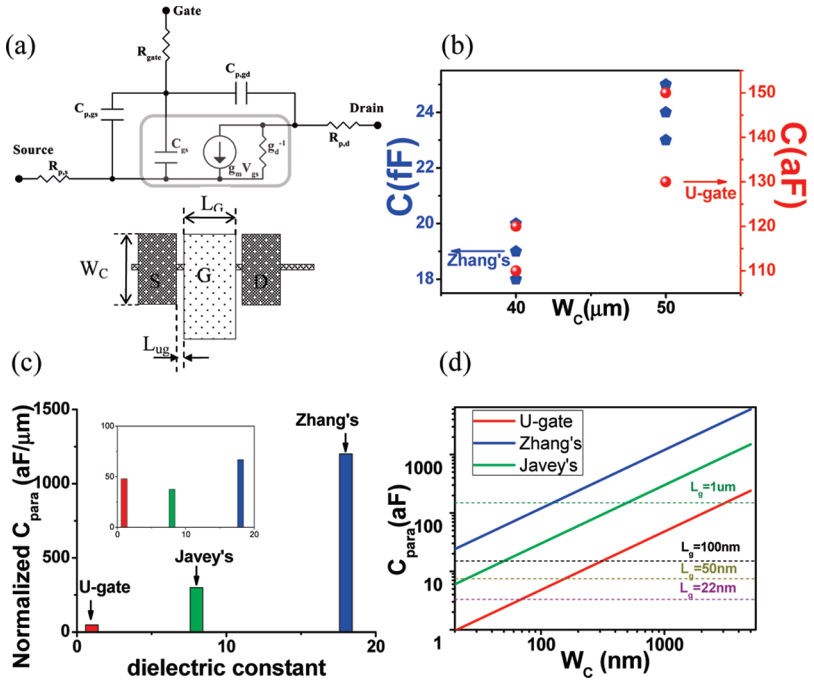

Figure 5. Circuit model and rf characteristics of three types of self-aligned CNT FET structures. (a) Small-signal equivalent circuit model (top) and general planform of a CNT FET (bottom). (b) Structure capacitance with the source/drain width being 40 and 50 μm for Zhang's structure (blue pentagons) and U-gate structure (red balls). (c) Normalized (by a space of 5 nm from the source/drain to the gate) structure capacitance *vs* dielectric constant for three types self-aligned device structures per μm contact width. Inset: Comparison of structure capacitance between three types of self-aligned structures further normalized by a dielectric constant. (d) Relationship between structure capacitance and contact width for three types of self-aligned device structures. The horizontal dotted lines denote the intrinsic gate capacitance of the CNT FETs with gate length being 1 μm, 100 nm, 50 nm, and 22 nm, respectively, from top to bottom. The gate capacitance per gate length is set as a typical value of 1.5 pF/cm.

classic electrostatic theory for a given device geometry. Therefore the effective cutoff frequency may be obtained indirectly using eq 1 as soon as the parasitic capacitances $C_{p,gd}$ and $C_{p,gs}$ are known, and these quantities may be measured as we will consider below.

The planform of the self-aligned device structure is depicted in the lower part of Figure 5a. Since the parasitic capacitances $C_{p,gd}$ and $C_{p,gs}$ are very small, to accurately measure them we fabricated SA gate structures with a very large W_c of about 40−50 μm but without the CNT channel to exclude the effect of the intrinsic gate capacitance with the CNT channel. We measured the total parasitic capacitance C_{para} (= $C_{p,gs}$ + $C_{p,gd}$) with the source and drain being connected as the common electrode and the gate as the other electrode, and the obtained values of C_{para} for the U-gate and Zhang's SA structure[9] are compared with varying W_c as shown in Figure 5b. The detailed method to measure parasitic capacitance was described in the Experimental Section and the Supporting Information. It is obvious that the parasitic capacitance of the U-gate structure is nearly 2 orders of magnitudes smaller than that of Zhang's SA structure with the same contact width W_c. The total parasitic capacitances normalized by the contact width W_c are about 3 aF/μm for the U-gate structure and 500 aF/μm for Zhang's SA structure, while the corresponding value is about 300 aF/μm for Javey's SA structure.[14] Since the three types of structures are unfairly compared with different ungated length L_{ug} (which are 80, 12, and 5 nm, respectively, for the three types of device structures), a further normalization should be carried out to make a fair comparison between different device structures. To a good approximation we assume that the parasitic capacitance is inversely proportional to the ungated channel length L_{ug}; relevant quantities are then scaled to the same L_{ug} value (here we set L_{ug} = 5 nm) to yield a normalized parasitic capacitance of 48 aF/μm for the U-gate structure and 1200 and 300 aF/μm respectively for Zhang's and Javey's SA structures as shown in Figure 5c. The U-gate CNT FET thus has a much smaller parasitic capacitance than that of the other two types of SA devices with the same contact width W_c and ungated length L_{ug}. If we further scale the total parasitic capacitance with the relative dielectric constant of the insulator filling the space between the source/drain and gate, the final normalized C_{para} converges to the same order of magnitude for all three types of SA structures as shown in the inset of Figure 5c. The remaining difference might come from the thickness disparity of the electrodes. We therefore conclude that the significantly reduced parasitic capacitance of the U-gate device originates mainly from replacing the high-κ dielectric material between the source/drain

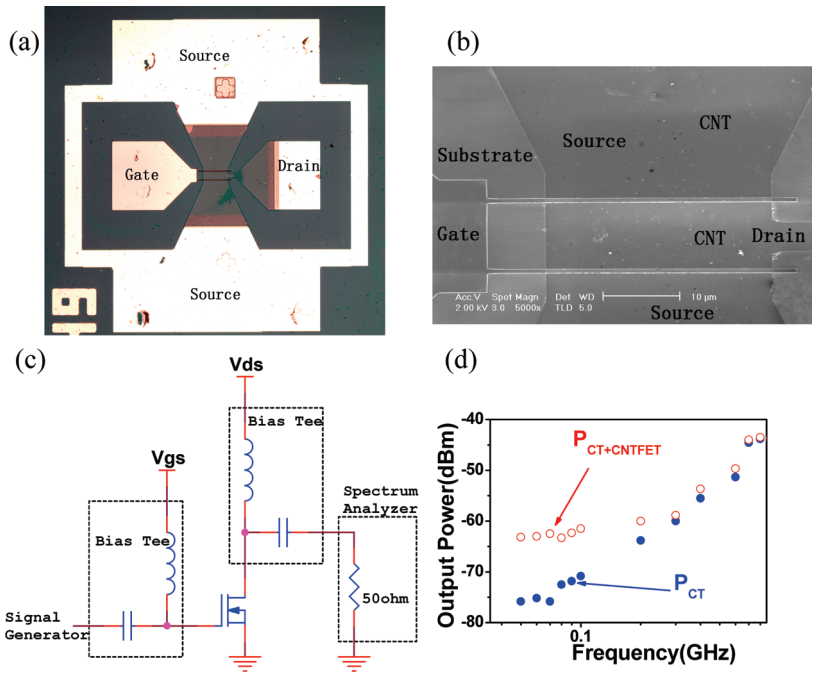

Figure 6. Radio frequency characteristics of the self-aligned U-gate CNT FETs. (a) Photo image of a real device with GSG pads. (b) SEM picture of the device with a gate length of 0.6 μm and contact width of 30 μm. (c) Experimental setup used to measure the frequency response of the self-aligned U-gate CNT FET. (d) Measured values of the crosstalk power P_{CT} and the total power $P_{CT+CNTFET}$ for the self-aligned U-gate CNT FETs for V_{gs} = 0.5 V and V_{ds} = 0.5 V. The input power is −10 dBm.

and gate electrodes in the other two self-aligned device structures by a vacant space with $\kappa \approx 1$.

The shrinkage of the parasitic capacitance will provide a larger space for designing the layout of the CNT FET for high-speed integrated circuits. To increase the speed (benchmarked by the cutoff frequency) of the CNT FET, we should scale down the gate length L_g to increase the transconductance g_m and to reduce the parasitic capacitance C_{para} of the device accordingly. If the parasitic capacitance C_{para} is not larger than the gate capacitance, we consider the structure to be a good one such that its effective cutoff frequency is at least larger than 50% of the intrinsic cutoff frequency (see for example eq 1). The most straightforward way to reduce the parasitic capacitance is to shrink the contact width W_c. This is because the parasitic capacitance depends linearly on the contact width (Figure 5d). For the convenience of our following discussions, we refer to the contact width W_c as the optimized one when the corresponding parasitic capacitance C_{para} is equal to the intrinsic gate capacitance C_{gs}. The intrinsic gate capacitance of a self-aligned CNT FET is typically about 1.5 pF/cm;[9−12] then C_{gs} is about 150, 15, 7.5, and 3.3 aF, respectively, for L_g = 1 μm, 100 nm, 50 nm, and 22 nm, as indicated by the horizontal dashed lines from top to bottom in Figure 5d. It is obvious that for a device with L_g = 1 μm the optimized contact width should be smaller than about 3 μm with the U-gate structure, while the corresponding values are respectively 500 and 120 nm with Javey's and Zhang's SA structures. This means that there is more room for optimizing the layout of the device if the SA U-gate structure is adopted than that using Javey's and Zhang's SA structures. In particular when the gate length is scaled down to 22 nm, *i.e.*, the characteristic dimension of the next generation Si-based CMOS devices,[22] the optimized contact width should be smaller than about 70 nm with the U-gate structure. If Javey's and Zhang's SA structures are used, the optimized contact width should be smaller than 10 nm, which is beyond the reach of the conventional fabrication technique. This is because it is almost impossible to fabricate so narrow a metal line and to align it accurately on top of the CNT channel. In principle, the U-gate structure can also be used in FETs with an array of parallel CNTs or CNT network as the channel to further optimize their rf properties.

The frequency response of the self-aligned U-gate CNT FETs was assessed *via* a direct ac measurement, which is usually referred to as large-signal frequency-domain measurements.[28,29] Figure 6a and b show the geometry of the final device for high-frequency measurement. The setup used to measure the frequency response of CNT FETs is shown in Figure 6c, in which a signal generator is used to apply a sine wave and a spectrum analyzer is used to measure the output crosstalk signal. The measured results are shown in Figure 6d, in which $P_{CT+CNTFET}$ is the total signal power and P_{CT} is the crosstalk power with CNT FET being off. At low frequency (less than 200 MHz) $P_{CT+CNTFET}$ is far beyond P_{CT}. But as the input frequency increases, $P_{CT+CNTFET}$ and P_{CT} are

approaching each other and almost coincide at about 800 MHz. Since the coincidence between $P_{CT+CNTFET}$ and P_{CT} suggests that the CNT FET does not work any longer, the cutoff frequency of the device is estimated to be about 800 MHz.[28] It should be noted that this cutoff measured from our SA U-gate device is much higher than any of the previously reported values for FETs fabricated on a single CNT through a direct measurement method.[28,29] In principle both the contact width and channel length can be reduced, and the large parasitic capacitance is due to the silicon substrate used in this work, which can be eliminated by replacing the silicon substrate with a more insulating one. We expect that the cutoff frequency f_T may be significantly improved by further optimization of the device geometry.

In conclusion, we have introduced a novel self-aligned U-gate structure and shown that the U-gate CNT FET exhibits excellent dc and rf performance simultaneously. In particular, the U-gate CNT FET shows a subthreshold swing of about 75 mV/dec and a practically zero DIBL, indicating that the electrostatic potential of the whole CNT channel is efficiently controlled by the U-gate and that the device is a well-behaved FET. Moreover the rf properties of the device are assessed in detail by analyzing the parasitic capacitance, which is measured by an ultraprecision capacitance bridge and shown to be much smaller than all previously developed self-aligned device structures. This significant shrinkage in the parasitic capacitance thus provides more space for designing next generation high-speed integrated circuits. Direct ac frequency domain measurements on the SA U-gate CNT FETs also resulted in a much higher cutoff frequency of 800 MHz than previously reported values.

EXPERIMENTAL SECTION

Fabrication of U-Gate CNT FETs. The ultralong CNT used in this work is of about one millimeter long and is grown by catalytic chemical vapor deposition[23] on a heavily n-doped silicon wafer that is covered with a 500 nm thermally grown SiO_2. Field-effect measurement was carried out to determine whether the CNT is semiconducting or metallic. The heavily n-doped silicon wafer was used as the back gate, and measurement pads and the source/drain were fabricated by electron beam lithography (EBL). This U-gate CNT FET was fabricated *via* two simple steps of EBL. First, a bilayer resist process of copolymer/PMMA 950K was used. The two layers of resist were both spun at 6000 rpm for 1 min and baked for 3 min at 180 °C on a hot plate. It is well known that two different kinds of resist will dissolve into each other without a barrier layer between them such that the sensitivity of the bilayer resist varies continuously from top (high sensitivity) to bottom (low sensitivity). Figure 1a shows an idealized resist profile after the process. A 3 nm layer of Y was deposited by e-beam evaporation and oxidized by UVO[24] for 5 min to yield a gate dielectric layer Y_2O_3 of 6.5 nm, as shown in Figure 1b. A 70 nm gate metal layer of Ti was then deposited on top of the Y_2O_3 layer as shown in Figure 1c, and the geometry of the final gate stack is sketched in Figure 1d. The two ends of the top-gate stack bend upward, leaving two vacant spaces between the U-shaped top-gate and the nearby source/drain electrodes. Second, windows for defining the source/drain were patterned by a monolayer resist process of PMMA 200K and EBL without precise alignment (Figure 1e). The source/drain electrodes were formed by direct deposition of Sc (20 nm) using the top-gate stack as the mask. The source/drain electrodes are seen to automatically separate from the top-gate stack by a distance L_{ug}, and in this article we refer to this region as "ungated" (not directly by the top-gate, Figure 1f). Depicted in Figure 1g is the final geometry of the U-shaped top-gate CNT FET, and shown in Figure 1f is a SEM image of a typical device with L_{ug} = 80 nm and θ = 60°. Experimentally, both L_{ug} and θ can be controlled by carefully choosing the thickness and sensitivity of the bilayer resist.

Measurement of the Parasitic Structure Capacitances. The U-shaped and Zhang's self-aligned structures were respectively fabricated on SiO_2/Si wafers with same gate length and two sets of source/drain electrode widths, *i.e.*, 40 and 50 μm. In the U-shaped gate structure, the ungated length L_{ug} is 80 nm and the space between the source/drain and gate is vacant. In Zhang's SA structure, L_{ug} = 12 nm and the space between the source/drain and gate is filled with ALD-growth HfO_2 with a dielectric constant of about 18. In this work source and drain electrodes are linked together to measure the total parasitic capacitance ($C_{para} = C_{p,gs} + C_{p,ds}$). The capacitance measurements are performed with an ultraprecision capacitance bridge (Andeen-Hagerling, model 2700A, and the detailed principle is described in the Supporting Information) in a variable-temperature cryogenic probe station (Lakeshore). AH 2007A and probe station are connected by BNC wires, and two probes are used for the gate and source/drain separately. This measurement scheme is widely used by many groups for small capacitance acquisition of different materials.[25−27]

Frequency Measurement Method. For rf measurement, the U-gate self-aligned device is fabricated with GSG pads (Figure 6a) with a gate length of 0.6 μm and contact width of 30 μm, respectively. The pads for measurement are made of metal stacks, which are titanium and gold. The GSG center departure is 150 μm. Figure 6c shows the instrumental setup used to measure the frequency response of our U-gate self-aligned device using a spectrum analyzer. Direct current biases of the device are provided with Bias Tee. The gate is biased about 0.5 V to operate at the midpoint of the drain current output, and a signal generator was used to apply a sine wave (the input power is about −10 dBm). The U-gate self-aligned device response is observed on the spectrum analyzer and measured as a function of frequency by varying the input frequency from 50 to 900 MHz.

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Supporting Information Available: Additional experimental details. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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